CLAIMS

What is claimed is:

1. A method that constrains a DC level of an input word, comprising:

dividing said input word into a plurality of components, wherein said components include n symbols;

summing said n symbols of said components and generating a sum for each component;

comparing an absolute value of said sum to a threshold;

encoding said component into a substitute component if said absolute value of said sum for said component exceeds said threshold; and

combining said components having said sum with said absolute value that does not exceed said threshold with at least one substitute component into an output word.

2. The method of claim 1 wherein said substitute component includes less than n symbols.

3. The method of claim 1 wherein said input word includes 32 symbols and said output word includes at least 33 symbols.

4. The method of claim 3 wherein said components include 8 symbols and wherein said threshold is 4.

5. The method of claim 4 wherein said substitute component includes 5 symbols.

6. The method of claim 1 further comprising selecting an output word template based on a number of substitute components and based on a position that said substitute components originally occupied in said input word.

7. The method of claim 6 further comprising inserting said substitute components in said output word based on said output word template.

8. The method of claim 7 further comprising inserting said components that have said sum with said absolute value that does not exceed said threshold in said output word based on said output word template.

9. The method of claim 8 further comprising inserting address symbols in said output word based on said output word template.

10. The method of claim 9 further comprising inserting indicator symbols in said output word based on said output word template.

11. The method of claim 1 further comprising adding a parity symbol to said output word to make a product of symbols of said output word positive.

12. The method of claim 1 further comprising adding a parity symbol to said output word to make a product of symbols of said output word negative.

13. The method of claim 1 wherein said symbols are in an alphabet {1, -1}.

14. The method of claim 1 wherein said output word has a sum between -17 and 17.

15. The method of claim 1 further comprising encoding said component into a substitute component if said symbols of said component alternate between a positive value and a negative value over said n symbols.

16. The method of claim 1 further comprising encoding said component into a substitute component if said symbols of said component alternate between a negative value and a positive value over said n symbols.

17. A method that constrains a DC level of an input word for a perpendicular recorder that records symbols on a magnetic media, comprising:

dividing said input word into a plurality of components, wherein said components include n symbols;

summing said n symbols of said components and generating a sum for each component;

comparing an absolute value of said sum to a threshold;

encoding said component into a substitute component having fewer than n symbols if said absolute value of said sum for said component exceeds said threshold;

combining said components having said sum with said absolute value that does not exceed said threshold with at least one substitute component into an output word, wherein said substitute components reduce a digital sum of said symbols of said input word; and

writing said output word using said perpendicular recorder on said magnetic media.

18. The method of claim 17 wherein said input word includes 32 symbols and said output word includes at least 33 symbols.

19. The method of claim 18 wherein said components include 8 symbols and said threshold is equal to 4.

20. The method of claim 19 wherein said substitute component includes 5 symbols.

21. The method of claim 17 further comprising selecting an output word template based on a number of substitute components and based on a position that said substitute components originally occupied in said input word.

22. The method of claim 21 further comprising inserting said substitute components in said output word based on said output word template.

23. The method of claim 22 further comprising inserting said components that have said sum with said absolute value that does not exceed said threshold in said output word based on said output word template.

24. The method of claim 23 further comprising inserting address symbols in said output word based on said output word template.

25. The method of claim 24 further comprising inserting indicator symbols in said output word based on said output word template.

26. The method of claim 17 further comprising adding a parity symbol to said output word to make a product of symbols of said output word positive.

27. The method of claim 17 further comprising adding a parity symbol to said output word to make a product of symbols of said output word negative.

28. The method of claim 17 wherein said output word has a sum between -17 and 17.

29. The method of claim 17 further comprising encoding said component into a substitute component if said symbols of said component alternate between a positive value and a negative value over said n symbols.

30. The method of claim 17 further comprising encoding said component into a substitute component if said symbols of said component alternate between a negative value and a positive value over said n symbols.

31. A DC-level constraining circuit that constrains a DC level of an input word, comprising:

dividing means for dividing said input word into a plurality of components, wherein said components include n symbols;

summing means for summing said n symbols of said components and for generating a sum for each component;

comparing means for comparing an absolute value of said sum to a threshold;

encoding means for encoding said component into a substitute component if said absolute value of said sum for said component exceeds said threshold; and

combining means for combining said components having said sum with said absolute value that does not exceed said threshold with at least one substitute component into an output word.

32. The DC-level constraining circuit of claim 31 wherein said substitute component includes less than n symbols.

33. The DC-level constraining circuit of claim 31 wherein said input word includes 32 symbols and said output word includes at least 33 symbols.

34. The DC-level constraining circuit of claim 33 wherein said components include 8 symbols and wherein said threshold is 4.

35. The DC-level constraining circuit of claim 34 wherein said substitute component includes 5 symbols.

36. The DC-level constraining circuit of claim 31 wherein said encoding means selects an output word template based on a number of substitute components and based on a position that said substitute components originally occupied in said input word.

37. The DC-level constraining circuit of claim 36 wherein said encoding means inserts said substitute components in said output word based on said output word template.

38. The DC-level constraining circuit of claim 37 wherein said encoding means inserts said components that have said sum with said absolute value that does not exceed said threshold in said output word based on said output word template.

39. The DC-level constraining circuit of claim 38 wherein said encoding means inserts address symbols in said output word based on said output word template.

40. The DC-level constraining circuit of claim 39 wherein said encoding means inserts indicator symbols in said output word based on said output word template.

41. The DC-level constraining circuit of claim 31 further comprising parity means for adding a parity symbol to said output word to make a product of symbols of said output word positive.

42. The DC-level constraining circuit of claim 31 further comprising parity means for adding a parity symbol to aid output word to make a product of symbols of said output word negative.

43. The DC-level constraining circuit of claim 31 wherein said symbols are in an alphabet {1, -1}.

44. The DC-level constraining circuit of claim 31 wherein said output word has a sum between -17 and 17.

45. The DC-level constraining circuit of claim 31 wherein said encoding means encodes said component into a substitute component if said symbols of said component alternate between a positive value and a negative value over said n symbols.

46. The DC-level constraining circuit of claim 31 wherein said encoding means encodes said component into a substitute component if said symbols of said component alternate between a negative value and a positive value over said n symbols.

47. A DC-level constraining circuit that constrains a DC level of an input word for a perpendicular recorder that records symbols on a magnetic media, comprising:

dividing means for dividing said input word into a plurality of components, wherein said components include n symbols;

summing means for summing said n symbols of said components and for generating a sum for each component;

comparing means for comparing an absolute value of said sum to a threshold;

encoding means for encoding said component into a substitute component having fewer than n symbols if said absolute value of said sum for said component exceeds said threshold;

combining means for combining said components having said sum with said absolute value that does not exceed said threshold with at least one substitute component into an output word, wherein said substitute components reduce a digital sum of said symbols of said input word; and

writing said output word using said perpendicular recorder on said magnetic media.

48. The DC-level constraining circuit of claim 47 wherein said input word includes 32 symbols and said output word includes at least 33 symbols.

49. The DC-level constraining circuit of claim 48 wherein said components include 8 symbols and said threshold is equal to 4.

50. The DC-level constraining circuit of claim 49 wherein said substitute component includes 5 symbols.

51. The DC-level constraining circuit of claim 47 wherein said encoding means selects an output word template based on a number of substitute components and based on a position that said substitute components originally occupied in said input word.

52. The DC-level constraining circuit of claim 51 wherein said encoding means inserts said substitute components in said output word based on said output word template.

53. The DC-level constraining circuit of claim 52 wherein said encoding means inserts said components that have said sum with said absolute value that does not exceed said threshold in said output word based on said output word template.

54. The DC-level constraining circuit of claim 53 wherein said encoding means inserts address symbols in said output word based on said output word template.

55. The DC-level constraining circuit of claim 54 wherein said encoding means inserts indicator symbols in said output word based on said output word template.

56. The DC-level constraining circuit of claim 47 further comprising parity means for adding a parity symbol to said output word to make a product of symbols of said output word positive.

57. The DC-level constraining circuit of claim 47 further comprising parity means for adding a parity symbol to said output word to make a product of symbols of said output word negative.

58. The DC-level constraining circuit of claim 57 wherein said output word has a sum between -17 and 17.

59. The DC-level constraining circuit of claim 57 wherein said encoding means encodes said component into a substitute component if said symbols of said component alternate between a positive value and a negative value over said n symbols.

60. The DC-level constraining circuit of claim 57 wherein said encoding means encodes said component into a substitute component if said symbols of said component alternate between a negative value and a positive value over said n symbols.

61. A DC-level constraining circuit that constrains a DC level of an input word, comprising:

a divider that divides said input word into a plurality of components, wherein said components include n symbols;

a summer that sums said n symbols of said components and generates a sum for each component;

a comparator that compares an absolute value of said sum to a threshold; and

an encoder that encodes said component into a substitute component if said absolute value of said sum for said component exceeds said threshold and combines said components having said sum with said absolute value that does not exceed said threshold with at least one substitute component into an output word.

62. The DC-level constraining circuit of claim 61 wherein said substitute component includes less than n symbols.

63. The DC-level constraining circuit of claim 61 wherein said input word includes 32 symbols and said output word includes at least 33 symbols.

64. The DC-level constraining circuit of claim 63 wherein said components include 8 symbols and wherein said threshold is 4.

65. The DC-level constraining circuit of claim 64 wherein said substitute component includes 5 symbols.

66. The DC-level constraining circuit of claim 61 wherein said encoder selects an output word template based on a number of substitute components and based on a position that said substitute components originally occupied in said input word.

67. The DC-level constraining circuit of claim 66 wherein said encoder inserts said substitute components in said output word based on said output word template.

68. The DC-level constraining circuit of claim 67 wherein said encoder inserts said components that have said sum with said absolute value that does not exceed said threshold in said output word based on said output word template.

69. The DC-level constraining circuit of claim 68 wherein said encoder inserts address symbols in said output word based on said output word template.

70. The DC-level constraining circuit of claim 69 wherein said encoder inserts indicator symbols in said output word based on said output word template.

71. The DC-level constraining circuit of claim 61 further comprising a parity coder that adds a parity symbol to said output word to make a product of symbols of said output word positive.

72. The DC-level constraining circuit of claim 61 further comprising a parity coder that adds a parity symbol to said output word to make a product of symbols of said output word negative.

73. The DC-level constraining circuit of claim 61 wherein said symbols are in an alphabet {1, -1}.

74. The DC-level constraining circuit of claim 61 wherein said output word has a sum between -17 and 17.

75. The DC-level constraining circuit of claim 61 wherein said encoder encodes said component into a substitute component if said symbols of said component alternate between a positive value and a negative value over said n symbols.

76. The DC-level constraining circuit of claim 61 wherein said encoder encodes said component into a substitute component if said symbols of said component alternate between a negative value and a positive value over said n symbols.

77. A DC-level constraining circuit that constrains a DC level of an input word for a perpendicular recorder that records symbols on a magnetic media, comprising:

a divider that divides said input word into a plurality of components, wherein said components include n symbols;

a summer that sums said n symbols of said components and generates a sum for each component;

a comparator that compares an absolute value of said sum to a threshold;

an encoder that encodes said component into a substitute component having fewer than n symbols if said absolute value of said sum for said component exceeds said threshold and that combines said components having said sum with said absolute value that does not exceed said threshold with at least one substitute component into an output word, wherein said substitute components reduce a digital sum of said symbols of said input word; and

a perpendicular recorder that writes said output word on said magnetic media.

78. The DC-level constraining circuit of claim 77 wherein said input word includes 32 symbols and said output word includes at least 33 symbols.

79. The DC-level constraining circuit of claim 78 wherein said components include 8 symbols and said threshold is equal to 4.

80. The DC-level constraining circuit of claim 79 wherein said substitute component includes 5 symbols.

81. The DC-level constraining circuit of claim 77 wherein said encoder selects an output word template based on a number of substitute components and based on a position that said substitute components originally occupied in said input word.

82. The DC-level constraining circuit of claim 81 wherein said encoder inserts said substitute components in said output word based on said output word template.

83. The DC-level constraining circuit of claim 82 wherein said encoder inserts said components that have said sum with said absolute value that does not exceed said threshold in said output word based on said output word template.

84. The DC-level constraining circuit of claim 83 wherein said encoder inserts address symbols in said output word based on said output word template.

85. The DC-level constraining circuit of claim 84 wherein said encoder inserts indicator symbols in said output word based on said output word template.

86. The DC-level constraining circuit of claim 77 further comprising a parity coder that adds a parity symbol to said output word to make a product of symbols of said output word positive.

87. The DC-level constraining circuit of claim 77 further comprising a parity coder that adds a parity symbol to said output word to make a product of symbols of said output word negative.

88. The DC-level constraining circuit of claim 87 wherein said output word has a sum between -17 and 17.

89. The DC-level constraining circuit of claim 87 wherein said encoder encodes said component into a substitute component if said symbols of said component alternate between a positive value and a negative value over said n symbols.

90. The DC-level constraining circuit of claim 87 wherein said encoder encodes said component into a substitute component if said symbols of said component alternate between a negative value and a positive value over said n symbols.

91. A method for decoding an output word of DC-level constraining encoder, comprising:

identifying address and indicator symbols in said output word;

selecting an output word template based on said address and indicator symbols; and

using said output word template to identify good components and substitute components in said output word.

92. The method of claim 91 further comprising decoding said substitute components into bad components.

93. The method of claim 92 further comprising combining said good components and said bad components into an input word.

94. The method of claim 91 further comprising removing a parity symbol from said output word.

95. The method of claim 93 wherein said output word has at least one of 33 and 34 symbols and said input word has 32 symbols.

96. A decoding circuit that decodes an output word of a DC-level constraining circuit, comprising:

identifying means for identifying address and indicator symbols in said output word; and

decoding means for selecting an output word template based on said address and indicator symbols and for using said output word template to identify good components and substitute components from said output word.

97. The decoding circuit of claim 96 wherein said decoding means decodes said substitute components into bad components.

98. The decoding circuit of claim 97 wherein said decoding means combines said good components and said bad components into an input word.

99. The decoding circuit of claim 96 further comprising parity means for removing a parity symbol from said output word.

100. The decoding circuit of claim 98 wherein said output word has at least one of 33 and 34 symbols and said input word has 32 symbols.

101. A decoding circuit that decodes an output word of DC-level constraining circuit, comprising:

an identifier that identifies address and indicator symbols in said output word; and

a decoder that selects an output word template based on said address and indicator symbols and that uses said output word template to extract good components and substitute components from said output word.

102. The decoding circuit of claim 101 wherein said decoder decodes said substitute components into bad components.

103. The decoding circuit of claim 102 wherein said decoder combines said good components and said bad components into an input word.

104. The decoding circuit of claim 101 further comprising a parity coder that removes a parity symbol from said output word.

105. The decoding circuit of claim 103 wherein said output word has at least one of 33 and 34 symbols and said input word has 32 symbols.

106. A DC-level constraining circuit that constrains a DC level of an input word, comprising:

an error correction coding (ECC) circuit;

an encoder that communicates with said ECC circuit, wherein said encoder divides said input word into a plurality of components each having n symbols, sums said n symbols of said components and generates a sum for each component, compares an absolute value of said sum to a threshold, encodes said component into a substitute component if said absolute value of said sum for said component exceeds said threshold, and combines said components having said sum with said absolute value that does not exceed said threshold with at least one substitute component into an output word; and

a disk drive that communicates with said encoder and that writes said output word onto a magnetic media.

107. The DC-level constraining circuit of claim 106 wherein said substitute component includes less than n symbols.

108. The DC-level constraining circuit of claim 106 wherein said input word includes 32 symbols and said output word includes at least 33 symbols.

109. The DC-level constraining circuit of claim 108 wherein said components include 8 symbols and wherein said threshold is 4.

110. The DC-level constraining circuit of claim 109 wherein said substitute component includes 5 symbols.

111. The DC-level constraining circuit of claim 106 wherein said encoder selects an output word template based on a number of substitute components and based on a position that said substitute components originally occupied in said input word.

112. The DC-level constraining circuit of claim 111 wherein said encoder inserts said substitute components in said output word based on said output word template.

113. The DC-level constraining circuit of claim 112 wherein said encoder inserts said components that have said sum with said absolute value that does not exceed said threshold in said output word based on said output word template.

114. The DC-level constraining circuit of claim 113 wherein said encoder inserts address symbols in said output word based on said output word template.

115. The DC-level constraining circuit of claim 114 wherein said encoder inserts indicator symbols in said output word based on said output word template.

116. The DC-level constraining circuit of claim 106 further comprising a parity coder that adds a parity symbol to said output word to make a product of symbols of said output word positive.

117. The DC-level constraining circuit of claim 106 further comprising a parity coder that adds a parity symbol to said output word to make a product of symbols of said output word negative.

118. The DC-level constraining circuit of claim 106 wherein said symbols are in an alphabet {1, -1}.

119. The DC-level constraining circuit of claim 106 wherein said output word has a sum between -17 and 17.

120. The DC-level constraining circuit of claim 106 wherein said encoder encodes said component into a substitute component if said symbols of said component alternate between a positive value and a negative value over said n symbols.

121. The DC-level constraining circuit of claim 106 wherein said encoder encodes said component into a substitute component if said symbols of said component alternate between a negative value and a positive value over said n symbols.

122. The DC-level constraining circuit of claim 106 wherein said disk drive is a perpendicular recorder.

123. A DC-level constraining circuit that constrains a DC level of an input word, comprising:

error means for providing error correction coding;

encoding means that communicates with said error means for dividing said input word into a plurality of components each having n symbols, for summing said n symbols of said components, for generating a sum for each component, for comparing an absolute value of said sum to a threshold, for encoding said component into a substitute component if said absolute value of said sum for said component exceeds said threshold, and for combining said components having said sum with said absolute value that does not exceed said threshold with at least one substitute component into an output word; and

drive means that communicates with said encoding means for writing said output word onto a magnetic media.

124. The DC-level constraining circuit of claim 123 wherein said substitute component includes less than n symbols.

125. The DC-level constraining circuit of claim 123 wherein said input word includes 32 symbols and said output word includes at least 33 symbols.

126. The DC-level constraining circuit of claim 125 wherein said components include 8 symbols and wherein said threshold is 4.

127. The DC-level constraining circuit of claim 126 wherein said substitute component includes 5 symbols.

128. The DC-level constraining circuit of claim 123 wherein said encoding means selects an output word template based on a number of substitute components and based on a position that said substitute components originally occupied in said input word.

129. The DC-level constraining circuit of claim 128 wherein said encoding means inserts said substitute components in said output word based on said output word template.

130. The DC-level constraining circuit of claim 129 wherein said encoding means inserts said components that have said sum with said absolute value that does not exceed said threshold in said output word based on said output word template.

131. The DC-level constraining circuit of claim 130 wherein said encoding means inserts address symbols in said output word based on said output word template.

132. The DC-level constraining circuit of claim 131 wherein said encoding means inserts indicator symbols in said output word based on said output word template.

133. The DC-level constraining circuit of claim 123 further comprising parity means for adding a parity symbol to said output word to make a product of symbols of said output word positive.

134. The DC-level constraining circuit of claim 123 further comprising parity means for adding a parity symbol to said output word to make a product of symbols of said output word negative.

135. The DC-level constraining circuit of claim 123 wherein said symbols are in an alphabet {1, -1}.

136. The DC-level constraining circuit of claim 123 wherein said output word has a sum between -17 and 17.

137. The DC-level constraining circuit of claim 123 wherein said encoding means encodes said component into a substitute component if said symbols of said component alternate between a positive value and a negative value over said n symbols.

138. The DC-level constraining circuit of claim 123 wherein said encoding means encodes said component into a substitute component if said symbols of said component alternate between a negative value and a positive value over said n symbols.

139. The DC-level constraining circuit of claim 123 wherein said drive means is a perpendicular recorder.

140. A method for constraining a DC level of an input word, comprising:

error correction coding an input word;

dividing said input word into a plurality of components each having n symbols;

summing said n symbols of said components and generating a sum for each component;

comparing an absolute value of said sum to a threshold;

encoding said component into a substitute component if said absolute value of said sum for said component exceeds said threshold;

combining said components having said sum with said absolute value that does not exceed said threshold with at least one substitute component into an output word; and

writing said output word onto a magnetic media.

141. The method of claim 140 wherein said substitute component includes less than n symbols.

142. The method of claim 140 wherein said input word includes 32 symbols and said output word includes at least 33 symbols.

143. The method of claim 142 wherein said components include 8 symbols and wherein said threshold is 4.

144. The method of claim 143 wherein said substitute component includes 5 symbols.

145. The method of claim 140 further comprising selecting an output word template based on a number of substitute components and based on a position that said substitute components originally occupied in said input word.

146. The method of claim 145 further comprising inserting said substitute components in said output word template based on said output word template.

147. The method of claim 146 further comprising inserting said components that have said sum with said absolute value that does not exceed said threshold in said output word based on said output word template.

148. The method of claim 147 further comprising inserting address symbols in said output word based on said output word template.

149. The method of claim 148 further comprising inserting indicator symbols in said output word based on said output word template.

150. The method of claim 140 further comprising adding a parity symbol to said output word to make a product of symbols of said output word positive.

151. The method of claim 140 further comprising adding a parity symbol to said output word to make a product of symbols of said output word negative.

152. The method of claim 140 wherein said symbols are in an alphabet {1, -1}.

153. The method of claim 140 wherein said output word has a sum between -17 and 17.

154. The method of claim 140 further comprising encoding said component into a substitute component if said symbols of said component alternate between a positive value and a negative value over said n symbols.

155. The method of claim 140 further comprising encoding said component into a substitute component if said symbols of said component alternate between a negative value and a positive value over said n symbols.

156. The method of claim 140 wherein said disk drive is a perpendicular recorder.

157. A DC-level constraining circuit that constrains a DC level of an input word, comprising:

an error correction coding (ECC) circuit;

an encoder that communicates with said ECC circuit, wherein said encoder divides said input word into a plurality of components each having n symbols, sums said n symbols of said components and generates a sum for each component, compares an absolute value of said sum to a threshold, encodes said component into a substitute component if said absolute value of said sum for said component exceeds said threshold, and combines said components having said sum with said absolute value that does not exceed said threshold with at least one substitute component into an output word; and

an output channel in communication with said encoder.

158. The DC-level constraining circuit of claim 157 wherein said output channel is one of an Ethernet, a wireless local area network, and a disk drive.

159. The DC-level constraining circuit of claim 157 wherein said substitute component includes less than n symbols.

160. The DC-level constraining circuit of claim 157 wherein said input word includes 32 symbols and said output word includes at least 33 symbols.

161. The DC-level constraining circuit of claim 160 wherein said substitute component includes 5 symbols.

162. The DC-level constraining circuit of claim 157 wherein said encoder selects an output word template based on a number of substitute components and based on a position that said substitute components originally occupied in said input word.

163. The DC-level constraining circuit of claim 162 wherein said encoder inserts said substitute components in said output word based on said output word template.

164. The DC-level constraining circuit of claim 163 wherein said encoder inserts said components that have said sum with said absolute value that does not exceed said threshold in said output word based on said output word template.

165. The DC-level constraining circuit of claim 164 wherein said encoder inserts address symbols in said output word based on said output word template.

166. The DC-level constraining circuit of claim 165 wherein said encoder inserts indicator symbols in said output word based on said output word template.

167. The DC-level constraining circuit of claim 157 further comprising a parity coder that adds a parity symbol to said output word to make a product of symbols of said output word positive.

168. The DC-level constraining circuit of claim 157 further comprising a parity coder that adds a parity symbol to said output word to make a product of symbols of said output word negative.

169. The DC-level constraining circuit of claim 157 wherein said symbols are in an alphabet {1, -1}.

170. The DC-level constraining circuit of claim 157 wherein said output word has a sum between -17 and 17.

171. The DC-level constraining circuit of claim 157 wherein said encoder encodes said component into a substitute component if said symbols of said component alternate between a positive value and a negative value over said n symbols.

172. The DC-level constraining circuit of claim 157 wherein said encoder encodes said component into a substitute component if said symbols of said component alternate between a negative value and a positive value over said n symbols.

173. The DC-level constraining circuit of claim 160 wherein said components include 8 symbols and wherein said threshold is 4.

174. A DC-level constraining circuit that constrains a DC level of an input word, comprising:

error means for providing error correction coding;

encoding means that communicates with said error means for dividing said input word into a plurality of components each having n symbols, for summing said n symbols of said components, for generating a sum for each component, for comparing an absolute value of said sum to a threshold, for encoding said component into a substitute component if said absolute value of said sum for said component exceeds said threshold, and for combining said components having said sum with said absolute value that does not exceed said threshold with at least one substitute component into an output word; and

an output channel in communication with said encoder.

175. The DC-level constraining circuit of claim 174 wherein said output channel is one of an Ethernet, a wireless local area network, and a disk drive.

176. The DC-level constraining circuit of claim 174 wherein said substitute component includes less than n symbols.

177. The DC-level constraining circuit of claim 174 wherein said input word includes 32 symbols and said output word includes at least 33 symbols.

178. The DC-level constraining circuit of claim 177 wherein said substitute component includes 5 symbols.

179. The DC-level constraining circuit of claim 174 wherein said encoding means selects an output word template based on a number of substitute components and based on a position that said substitute components originally occupied in said input word.

180. The DC-level constraining circuit of claim 179 wherein said encoding means inserts said substitute components in said output word based on said output word template.

181. The DC-level constraining circuit of claim 180 wherein said encoding means inserts said components that have said sum with said absolute value that does not exceed said threshold in said output word based on said output word template.

182. The DC-level constraining circuit of claim 181 wherein said encoding means inserts address symbols in said output word based on said output word template.

183. The DC-level constraining circuit of claim 182 wherein said encoding means inserts indicator symbols in said output word based on said output word template.

184. The DC-level constraining circuit of claim 174 further comprising parity means for adding a parity symbol to said output word to make a product of symbols of said output word positive.

185. The DC-level constraining circuit of claim 174 further comprising parity means for adding a parity symbol to said output word to make a product of symbols of said output word negative.

186. The DC-level constraining circuit of claim 174 wherein said symbols are in an alphabet {1, -1}.

187. The DC-level constraining circuit of claim 174 wherein said output word has a sum between -17 and 17.

188. The DC-level constraining circuit of claim 174 wherein said encoding means encodes said component into a substitute component if said symbols of said component alternate between a positive value and a negative value over said n symbols.

189. The DC-level constraining circuit of claim 174 wherein said encoding means encodes said component into a substitute component if said symbols of said component alternate between a negative value and a positive value over said n symbols.

190. The DC-level constraining circuit of claim 177 wherein said components include 8 symbols and wherein said threshold is 4.

191. A method for constraining a DC level of an input word, comprising:

error correction coding an input word;

dividing said input word into a plurality of components each having n symbols;

summing said n symbols of said components and generating a sum for each component;

comparing an absolute value of said sum to a threshold;

encoding said component into a substitute component if said absolute value of said sum for said component exceeds said threshold;

combining said components having said sum with said absolute value that does not exceed said threshold with at least one substitute component into an output word; and

transmitting said output word on an output channel.

192. The method of claim 191 wherein said output channel is one of an Ethernet, a wireless local area network, and a disk drive.

193. The method of claim 191 wherein said substitute component includes less than n symbols.

194. The method of claim 191 wherein said input word includes 32 symbols and said output word includes at least 33 symbols.

195. The method of claim 194 wherein said substitute component includes 5 symbols.

196. The method of claim 191 further comprising selecting an output word template based on a number of substitute components and based on a position that said substitute components originally occupied in said input word.

197. The method of claim 196 further comprising inserting said substitute components in said output word based on said output word template.

198. The method of claim 197 further comprising inserting said components that have said sum with said absolute value that does not exceed said threshold in said output word based on said output word template.

199. The method of claim 198 further comprising inserting address symbols in said output word based on said output word template.

200. The method of claim 199 further comprising inserting indicator symbols in said output word based on said output word template.

201. The method of claim 191 further comprising adding a parity symbol to said output word to make a product of symbols of said output word positive.

202. The method of claim 191 further comprising adding a parity symbol to said output word to make a product of symbols of said output word negative.

203. The method of claim 191 wherein said symbols are in an alphabet {1, -1}.

204. The method of claim 191 wherein said output word has a sum between -17 and 17.

205. The method of claim 191 further comprising encoding said component into a substitute component if said symbols of said component alternate between a positive value and a negative value over said n symbols.

206. The method of claim 191 further comprising encoding said component into a substitute component if said symbols of said component alternate between a negative value and a positive value over said n symbols.

207. The method of claim 194 wherein said components include 8 symbols and wherein said threshold is 4.

208. A decoding circuit for an encoded input word, comprising:

a preamplifier that communicates with a channel that carries an encoded output word;

a front end that communicates with said preamplifier;

a Viterbi coder that communicates with said front end;

a post processor that communicates with said Viterbi coder; and

a decoder that identifies address and indicator symbols in said output word, that selects an output word template based on said address and indicator symbols, and that uses said output word template to identify good components and substitute components in said encoded output word.

209. The decoding circuit of claim 208 wherein said channel is one of an Ethernet, a wireless local area network and a disk drive.

210. The decoding circuit of claim 208 wherein said decoder decodes said substitute components into bad components.

211. The decoding circuit of claim 210 wherein said decoder recombines said good components and said bad components into an input word.

212. The decoding circuit of claim 208 further comprising a parity circuit that removes a parity symbol from said output word.

213. The decoding circuit of claim 211 wherein said encoded output word has at least one of 33 symbols and said decoded input word has 32 symbols.

214. A decoding circuit for an encoded input word, comprising:

amplifying means that communicates with a channel that carries an encoded output word for amplifying said encoded output word;

front end means that communicates with said amplifying means and that processes said amplified and encoded output word;

coding means that communicates with said front end means for applying Viterbi coding;

processing means that communicates with said coding means for providing post processing; and

decoding means that communicates with said post processing means for identifying address and indicator symbols in said output word, for selecting an output word template based on said address and indicator symbols, and for using said output word template to identify good components and substitute components in said encoded output word.

215. The decoding circuit of claim 214 wherein said channel is one of an Ethernet, a wireless local area network and a disk drive.

216. The decoding circuit of claim 214 wherein said decoding means decodes said substitute components into bad components.

217. The decoding circuit of claim 216 wherein said decoding means recombines said good components and said bad components into an input word.

218. The decoding circuit of claim 214 further comprising parity means for removing a parity symbol from said output word.

219. The decoding circuit of claim 217 wherein said encoded output word has at least one of 33 symbols and said decoded input word has 32 symbols.

220. A method for decoding an encoded input word, comprising:

communicating with a channel that carries an encoded output word;

amplifying said encoded output word;

processing said amplified and encoded output word using a front end;

coding said amplified and encoded output word using Viterbi coding;

performing post processing;

identifying address and indicator symbols in said output word;

selecting an output word template based on said address and indicator symbols; and

using said output word template to identify good components and substitute components in said encoded output word.

221. The method of claim 220 wherein said channel is one of an Ethernet, a wireless local area network and a disk drive.

222. The method of claim 220 further comprising decoding said substitute components into bad components.

223. The method of claim 222 further comprising recombining said good components and said bad components into an input word.

224. The method of claim 220 further comprising removing a parity symbol from said output word.

225. The method of claim 223 wherein said encoded output word has at least one of 33 symbols and said input word has 32 symbols.

226. A software method that constrains a DC level of an input word, comprising:

dividing said input word into a plurality of components, wherein said components include n symbols;

summing said n symbols of said components and generating a sum for each component;

comparing an absolute value of said sum to a threshold;

encoding said component into a substitute component if said absolute value of said sum for said component exceeds said threshold; and

combining said components having said sum with said absolute value that does not exceed said threshold with at least one substitute component into an output word.

227. The software method of claim 226 wherein said substitute component includes less than n symbols.

228. The software method of claim 226 wherein said input word includes 32 symbols and said output word includes at least 33 symbols and wherein said components include 8 symbols and wherein said threshold is 4.

229. The software method of claim 226 further comprising writing said output word to an output media, wherein said output media is one of an Ethernet, a wireless local area network, and a disk drive.

230. The software method of claim 229 wherein said substitute component includes 5 symbols.

231. The software method of claim 226 further comprising selecting an output word template based on a number of substitute components and based on a position that said substitute components originally occupied in said input word.

232. The software method of claim 231 further comprising inserting said substitute components in said output word based on said output word template.

233. The software method of claim 232 further comprising inserting said components that have said sum with said absolute value that does not exceed said threshold in said output word based on said output word template.

234. The software method of claim 233 further comprising inserting address symbols in said output word based on said output word template.

235. The software method of claim 234 further comprising inserting indicator symbols in said output word based on said output word template.

236. The software method of claim 226 further comprising adding a parity symbol to said output word to make a product of symbols of said output word positive.

237. The software method of claim 226 further comprising adding a parity symbol to said output word to make a product of symbols of said output word negative.

238. The software method of claim 226 wherein said symbols are in an alphabet {1, -1}.

239. The software method of claim 226 wherein said output word has a sum between -17 and 17.

240. The software method of claim 226 further comprising encoding said component into a substitute component if said symbols of said component alternate between a positive value and a negative value over said n symbols.

241. The software method of claim 226 further comprising encoding said component into a substitute component if said symbols of said component alternate between a negative value and a positive value over said n symbols.

242. A software method that constrains a DC level of an input word for a perpendicular recorder that records symbols on a magnetic media, comprising:

dividing said input word into a plurality of components, wherein said components include n symbols;

summing said n symbols of said components and generating a sum for each component;

comparing an absolute value of said sum to a threshold;

encoding said component into a substitute component having fewer than n symbols if said absolute value of said sum for said component exceeds said threshold;

combining said components having said sum with said absolute value that does not exceed said threshold with at least one substitute component into an output word, wherein said substitute components reduce a digital sum of said symbols of said input word; and

writing said output word to an output media.

243. The software method of claim 242 wherein said input word includes 32 symbols and said output word includes at least 33 symbols and wherein said components include 8 symbols and said threshold is equal to 4.

244. The software method of claim 242 wherein said output media is one of an Ethernet, a wireless local area network, and a disk drive.

245. The software method of claim 243 wherein said substitute component includes 5 symbols.

246. The software method of claim 242 further comprising selecting an output word template based on a number of substitute components and based on a position that said substitute components originally occupied in said input word.

247. The software method of claim 246 further comprising inserting said substitute components in said output word based on said output word template.

248. The software method of claim 247 further comprising inserting said components that have said sum with said absolute value that does not exceed said threshold in said output word based on said output word template.

249. The software method of claim 248 further comprising inserting address symbols in said output word based on said output word template.

250. The software method of claim 249 further comprising inserting indicator symbols in said output word based on said output word template.

251. The software method of claim 242 further comprising adding a parity symbol to said output word to make a product of symbols of said output word positive.

252. The software method of claim 242 further comprising adding a parity symbol to said output word to make a product of symbols of said output word negative.

253. The software method of claim 242 wherein said output word has a sum between -17 and 17.

254. The software method of claim 242 further comprising encoding said component into a substitute component if said symbols of said component alternate between a positive value and a negative value over said n symbols.

255. The software method of claim 242 further comprising encoding said component into a substitute component if said symbols of said component alternate between a negative value and a positive value over said n symbols.